SEMICONDUCTOR DEVICE FABRICATION METHOD USING OXYGEN ION IMPLANTATION

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a semiconductor device fabrication method, more particularly to the isolation steps in the fabrication method.

2. Description of the Related Art

The most generally used method of isolating circuit elements in a semiconductor device has been local oxidation of silicon (LOCOS) and a variant of this method known as framed local oxidation of silicon (F-LOCOS). In a further variant, proposed in Japanese Unexamined Patent Application Publication No. 7-22504, oxygen ions are implanted into a silicon substrate to form a buried oxide layer (a pad oxide) while maintaining the monocrystalline structure of the silicon above, and this monocrystalline silicon is then selectively oxidized to form a field oxide with smooth transition or 'bird's-beak' regions.

Japanese Unexamined Patent Application Publication No. 6-310534 discloses another method in which an impurity of an opposite type to the source and drain type is implanted into the substrate after the field oxide has been formed. For an n-channel transistor, for example, ions of a p-type impurity such as boron (B^+) or boron difluoride (BF_2^+) may be implanted. This implantation determines the carrier density in the substrate, and thus the threshold voltage of the transistor, and avoids having the carrier density altered by the oxidation process that forms the field oxide. In particular, the impurity concentration near the interface between the active element region and the field oxide can be reliably controlled.

The LOCOS process and its variants do not work well in

devices with features as small as, for example 0.15 micrometer (0.15 μm). An alternative process that has come into use at these small geometries is shallow trench isolation (STI), but this process has turned out to be highly problematic when applied to devices having a silicon-on-insulator (SOI) structure, because it stresses the thin silicon layer, greatly degrading the electrical characteristics of the circuit elements formed therein. In particular, STI cannot be used in fully depleted SOI devices in which the silicon layer may be only forty nanometers (40 nm) thick, or less.

For SOI devices, accordingly, alternative isolation methods have been tried, such as the mesa isolation method, in which a thin layer of silicon is etched to form isolated mesas of silicon on an insulating layer. The etching process is illustrated in FIGs. 5A and 5B. An SOI substrate 200 comprising a silicon supporting layer 202, a buried oxide layer 204, and a silicon semiconductor layer 206 is covered with a photoresist film 212 which is patterned by photolithography as shown in FIG. 5A to define the mesa shapes. The silicon semiconductor layer 206 is then etched, the patterned photoresist functioning as an etching mask. FIG. 5B shows the adjacent parts of two mesas after the photoresist mask has been removed and the surface cleansed. The etching process also removes part of the buried oxide layer 204.

A problem with mesa isolation is that although the silicon semiconductor layer 206 may be thin, its thickness is not so small as to be entirely negligible, and the edges of the mesas are steep. The steep edges create problems in subsequent patterning processes, such as the patterning of gate electrodes by photolithography. In particular, extremely precise photolithography will be required for the formation of gate electrodes with gate lengths of 0.1 μm or

less. At these dimensions, the edges of the mesas cannot be ignored, especially since the etching process that forms the mesas increases the height of their edges by etching into the insulating layer 204 as well.

SUMMARY OF THE INVENTION

An object of the present invention is accordingly to provide a semiconductor device fabrication method that isolates circuit elements without creating a height difference between active regions and isolation regions, enabling fine patterns to be formed easily on the combined surface of the active and isolation regions.

Another object of the invention is to provide a semiconductor device fabrication method that can isolate circuit elements with finely patterned isolation regions.

The invented method is used to fabricate a semiconductor device having a silicon layer disposed on an insulating layer. After the silicon layer is formed, oxygen ions are implanted into selected parts thereof. These selected parts of the silicon layer are then oxidized to create isolation regions dividing the silicon layer into a plurality of mutually isolated active regions, in which circuit elements such as transistors can be formed.

An oxidation-resistant film such as a nitride film or a photoresist film may be formed on the silicon layer and used as a mask during the ion implantation and oxidation processes.

The oxidation process does not create steep vertical discontinuities between the active regions and isolation regions. Fine patterns can therefore be formed easily on the combined surface of the active and isolation regions.

Since oxygen ions have already been implanted into the silicon layer, the oxidation process proceeds quickly and is completed before extensive lateral oxidation can take place.

The transition zone between the isolation regions and active regions is therefore small; no pronounced bird's-beak is formed. This enables the active regions to be adequately isolated from one another by comparatively narrow, finely patterned isolation regions.

BRIEF DESCRIPTION OF THE DRAWINGS

In the attached drawings:

FIGs. 1A and 1B are sectional views illustrating two stages in the fabrication of a semiconductor device according to a first embodiment of the invention;

FIGs. 2A and 2B are sectional views illustrating two stages in the fabrication of a semiconductor device according to a second embodiment;

FIGs. 3A, 3B, and 3C are sectional views illustrating three stages in the fabrication of a semiconductor device according to a third embodiment;

FIG. 4 is a graph illustrating the oxygen ion concentration profile in a semiconductor device fabricated according to a fourth embodiment; and

FIGs. 5A and 5B are sectional views illustrating the conventional mesa isolation process.

DETAILED DESCRIPTION OF THE INVENTION

Embodiments of the invention will be described with reference to the drawings, in which like elements are indicated by like reference numerals.

FIGs. 1A and 1B illustrate the isolation steps in a first embodiment of the invention. An SOI substrate 100 comprising a silicon supporting substrate 102, a buried oxide layer 104, and a silicon layer 106 twenty to seventy nanometers thick is thermally oxidized to form a sacrificial oxide film or pad oxide film 108 five to fifty nanometers thick. This thermal oxidation process reduces the thickness

of the silicon layer 106 by an amount that can be precalculated; the thicknesses of the silicon layer 106 and pad oxide film 108 should be selected so that the remaining thickness of the silicon layer 106 and the thickness of the pad oxide film 108 are adequate for later fabrication steps. Next, a nitride film 110 ten to three hundred fifty nanometers thick is formed by chemical vapor deposition (CVD). The purpose of the pad oxide film 108 is to prevent direct contact between the silicon layer 106 and the nitride film 110. The surface of the nitride film 110 is then coated with a photoresist film 112, which is patterned by photolithography to define oxygen ion implantation regions. The nitride film 110 and photoresist film 112 are both oxidation-resistant. The nitride film 110 is then etched, the photoresist film 112 being used as a mask, to expose the pad oxide film 108 in the oxygen ion implantation areas. Depending on the ion implantation conditions, the pad oxide film 108 may also be etched, exposing the silicon layer 106. In FIG. 1A, the pad oxide film 108 is not etched. After the etching process, oxygen ions are implanted into the silicon layer 106, the nitride film 110 and photoresist film 112 both acting as masks. In FIG. 1A, the oxygen ions are implanted through the pad oxide film 108 with an accelerating voltage of, for example, five kilovolts (5 kV) and a concentration of 10^{14} ions/cm^2 into the region 114 of the silicon layer 106 disposed below the openings in the nitride film 110 and photoresist film 112.

Next, the photoresist film 112 is removed and a field oxidation process is carried out to form a field oxide film 116 as shown in FIG. 1B. The field oxide film 116 isolates different active regions of the silicon layer 106, in which circuit elements such as transistors will be formed in subsequent fabrication steps (not illustrated). The nitride film 110 and pad oxide film 108 are removed before the

circuit elements are formed.

The implantation of oxygen ions in FIG. 1A speeds the formation of the field oxide film 116 in FIG. 1B and reduces its lateral spread. Consequently, it is not necessary to allow an extra margin for a large bird's beak. Adequate isolation can therefore be obtained even if the field oxide film 116 is finely patterned and high levels of integration can be attained. The fabrication time can also be reduced, because of the rapid oxidation of the silicon layer 106. Moreover, since the silicon layer 106 is not etched, no steep vertical edges are formed, removing the problem found in mesa isolation.

The first embodiment is particularly advantageous for fully depleted silicon-on-insulator (FD-SOI) substrates in which the thickness of the silicon layer 106 is 70 nm or less, preferably 40 nm or less. The reason is that since the field oxidation process is completed quickly, it does not stress the thin silicon layer 106.

FIGs. 2A and 2B illustrate the isolation steps in a second embodiment of the invention. The second embodiment is identical to the first embodiment except that no nitride film is formed; the photoresist film 112 is applied directly to the pad oxide film 108. The photoresist film 112 acts as a mask during ion implantation in FIG. 2A, and during field oxidation in FIG. 2B.

Compared with the first embodiment, the second embodiment involves fewer process steps, since no nitride film is formed. The absence of the nitride film also prevents oxidation faults even if the isolation pattern is very fine. In the first embodiment, the oxidation resistance effect of the nitride film 110 extends into the edges of the region 114 in which the field oxide 116 will be formed, so oxidation faults may occur, especially if the openings in the nitride film 110 are very narrow. The second embodiment,

which uses only the photoresist film 112 as an oxidation mask, avoids such faults, even when the openings in the photoresist film 112 are narrow. The second embodiment thus enables the creation of finer field oxide patterns than in the first embodiment.

Even though there is no nitride film to prevent oxidation of unwanted areas, the pad oxide film 108 tends to prevent unwanted oxidation, by hindering the diffusion of oxygen into these areas. Moreover, due to the implantation of oxygen ions, the field oxidation process is completed quickly, as pointed out in the first embodiment, so any oxidation that may occur in unwanted areas will be slight. Under optimal oxidation conditions, the amount of unwanted oxide formed can be held to 10 nm or less, and the thickness of the silicon layer 106 can be chosen so that this amount of oxidation does not present a problem. For example, if the desired thickness of the silicon layer 106 after field oxidation is 40 nm, the process can be carried out so that the thickness of the silicon layer 106 before the isolation step is 50 nm.

FIGs. 3A to 3C illustrate the isolation steps in a third embodiment of the invention. The isolation process in the third embodiment begins as described in the first embodiment and proceeds in an identical manner through the etching of the nitride film 110. Next, the photoresist film 112 (shown in FIG. 1A) is removed and a nitride film is deposited on the entire surface. This nitride film is etched anisotropically, without a mask, leaving nitride sidewalls 118 on the inner walls of the openings in the nitride film 110, as shown in FIG. 3A. Oxygen ions are then implanted with an accelerating voltage of, for example, 5 kV and a concentration of 10^{14} ions/cm^2 into a region 114 in the silicon layer 106, the nitride film 110 and sidewalls 118 functioning as a mask, as indicated by the arrows in FIG. 3A.

Next the surface is cleansed if necessary, and field oxidation is carried out, forming a field oxide film 116 as shown in FIG. 3B. The nitride film 110 and pad oxide film 108 are then removed by any appropriate methods to complete the isolation process, as shown in FIG. 3C.

In the third embodiment, since the openings in the nitride film 110 are narrowed by the sidewalls 118, the region 114 into which oxygen ions are implanted is correspondingly reduced in size. Even if the ion implantation process or the field oxidation process involves a lateral spread in the silicon layer 106, the size of the field oxide film 116 remains comparable to or smaller than the size of the openings in the nitride film 110 defined by photolithography. The third embodiment thus permits the formation of very fine isolation patterns.

The sidewalls 118 of the third embodiment can also be formed when the pad oxide film 108 is absent as in the second embodiment.

The sidewalls 118 need not be formed from a nitride film; they can be formed from an oxide film instead.

FIG. 4 shows a preferred oxygen concentration profile for the oxygen implantation step in the first, second, and third embodiments. The vertical axis indicates implantation depth in nanometers, the depth increasing with increasing height on the axis. The dotted line 120 represents the interface between the silicon (Si) layer 106 and the buried oxide layer 104; the area below the dotted line 120 represents the thickness of the silicon layer 106. The horizontal axis indicates oxygen ion concentration in ions per square centimeter. The total number of ions implanted into the silicon layer 106 is, for example, 10^{14} to 10^{16} per square centimeter, but the concentration varies with depth in the silicon layer 106. The peak 122 of the concentration profile occurs at a depth deeper than the center 124 of the

silicon layer 106, in the part of the silicon layer 106 relatively near the buried oxide layer 104. As a result, during the field oxidation process, oxidation proceeds to the interface with the buried oxide layer 104, and the silicon layer 106 is adequately oxidized, even in the vicinity of this interface. Possible inadequate isolation due to inadequate oxidation of the silicon layer 106 is thereby avoided.

The method of implanting oxygen into the silicon layer 106 is not limited to the simple use of an accelerating voltage; other methods may be employed. For example, oxygen ions may be excited by plasma excitation, then directed by an electric field into the silicon layer 106.

The pad oxide film 108 or sacrificial oxide was described above as a thermal oxide film 5 to 50 nm thick, but an oxide film formed by chemical vapor deposition (CVD) can be used instead of a thermal oxide film. If a CVD film is used, then when the pad oxide film is removed after field oxidation, the removal process can be completed quickly, so that little of the field oxide film is lost. This simplifies the adjustment of the original thickness of the silicon layer.

The pad oxide film 108 may also be a combination of a thermal oxide film and a CVD film.

The oxygen implantation mask is not limited to the nitride film 110 and photoresist film 112 used in the embodiments above. For example, the pad oxide film may be used as an oxygen implantation mask, or a separate oxide film may be formed and used as a mask.

The invention has been described in the context of a fully depleted SOI device with a silicon layer thickness of, for example 20 to 70 nm, but the invention can also be applied to a partially depleted SOI device with a thicker silicon layer, or to a bulk device.

Those skilled in the art will recognize that further variations are possible within the scope of the invention, which is defined in the appended claims.